

CLAIMS

What is claimed is.

- 1 1. A computing system comprising:
2 a processor in a processor package;
3 a shunt, transient voltage regulator (STVR) in the processor package
4 and coupled to the processor; and
5 at least one input/output device coupled to at least one of the STVR
6 and the processor.

- 1 2. The computing system of claim 1, further including:
2 a decoupling capacitor coupled between the processor and the STVR.

- 1 3. The computing system of claim 1, further including:
2 at least one decoupling capacitor coupled between the processor and
3 the STVR, wherein the at least one decoupling capacitor is selected from a
4 land-side capacitor, a die-side capacitor, and a combination thereof.

- 1 4. The computing system of claim 1, further including:
2 an interposer coupled to the processor package; and
3 a decoupling capacitor in the interposer.

- 1 5. The computing system of claim 1, further including:
2 an interposer coupled to the processor package;
3 a first decoupling capacitor having a first capacitance functionality in
4 the interposer; and
5 coupled between the processor and the STVR, a second decoupling
6 capacitor having a second capacitance functionality that is different from the
7 first capacitance functionality.

1 6. The computing system of claim 1, further including:
2 an interposer that is integral with the processor package;
3 a first decoupling capacitor having a first capacitance functionality in
4 the interposer; and
5 coupled between the processor and the STVR, a second decoupling
6 capacitor having a second capacitance functionality different from the first
7 capacitance functionality.

1 7. The computing system of claim 1, further including:
2 a mounting substrate, wherein the processor package is coupled to
3 the mounting substrate; and
4 a DC power converter voltage regulator coupled to the processor in
5 series with the STVR.

1 8. The computing system of claim 1, further including:
2 a mounting substrate, wherein the processor package is coupled to
3 the mounting substrate;
4 a power socket between the processor and the mounting substrate;
5 and
6 a DC power converter voltage regulator on the mounting substrate
7 and coupled to the processor in series with the STVR.

1 9. The computing system of claim 1, further including:
2 a mounting substrate, wherein the processor package is coupled to
3 the mounting substrate; and
4 a DC power converter voltage regulator coupled to the processor in
5 series with the STVR, wherein the DC power converter voltage regulator is
6 optimized for DC power conversion.

1 10. The computing system of claim 1, wherein the STVR is optimized
2 for responding to a processor load transient.

1 11. The computing system of claim 1, wherein the computing system is
2 disposed in one of a computer, a wireless communicator, a hand-held device, an
3 automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

1 12. The computing system of claim 1, wherein an STVR is coupled to at
2 least one of data storage, a digital signal processor, an application-specific
3 integrated circuit, and a microcontroller.

1 13. An apparatus comprising:
2 a processor package including:
3 a processor; and
4 a shunt, transient voltage regulator (STVR);
5 a mounting substrate, wherein the processor is coupled to the
6 mounting substrate;
7 a DC power converter coupled in series with the STVR, to the
8 processor; and
9 at least one input/output device coupled to at least one of the STVR
10 and the processor.

1 14. The apparatus of claim 13, further including:
2 coupled between the processor and the STVR, a decoupling
3 capacitor.

1 15. The apparatus of claim 13, further including:
2 an interposer coupled to the processor package;
3 in the interposer, a first decoupling capacitor having a first
4 capacitance functionality; and

5 coupled between the processor and the STVR, a second decoupling
6 capacitor having a second capacitance functionality that is different from the
7 first capacitance functionality.

1 16. The apparatus of claim 13, further including:
1 between the processor and the mounting substrate, a power socket;
2 and
3 coupled between the processor and the STVR, a decoupling capacitor
4 in an interposer.

1 17. The apparatus of claim 13, wherein the apparatus is disposed in one
2 of a computer, a wireless communicator, a hand-held device, an automobile, a
3 locomotive, an aircraft, a watercraft, and a spacecraft.

1 18. The apparatus of claim 13, wherein an STVR is coupled to at least
2 one of data storage, a digital signal processor, an application-specific integrated
3 circuit, and a microcontroller.

1 19. A method comprising:
2 operating a processor in a processor package, wherein the processor
3 package is coupled to at least one of an input/output device; and
4 with a shunt, transient voltage regulator (STVR) in the processor
5 package, responding to transient loads of the processor.

1 20. The method of claim 19, wherein the STVR is operated with an
2 independent voltage source first shunt, and a ground second shunt.

1 21. The method of claim 19, further including:
2 with a DC voltage converter spaced apart from the processor
3 package, converting at least one voltage input to Vcc.

1 22. The method of claim 19, further including:
2 responding to all processor transients with decoupling capacitor functionality
3 selected from a second decoupling capacitor in the processor package, a first
4 decoupling capacitor in an interposer that is coupled to the processor package, a first
5 decoupling capacitor in an interposer that is integral with the processor package, and
6 a combination thereof.

1 23. The method of claim 19, wherein the STVR includes an independent
2 voltage source first shunt and a ground second shunt, and further including:
3 controlling the first shunt and the second shunt by gated logic.

1 24. A method comprising:
2 inserting a shunt, transient voltage regulator (STVR) in a processor
3 package; and
4 coupling the processor package to at least one of an input/output
5 device.

1 25. The method of claim 24, further including:
2 on a mounting substrate for the processor package, coupling in series
3 a DC voltage converter to the STVR.

1 26. The method of claim 24, wherein the STVR includes an independent
2 voltage source first shunt, and a ground second shunt.

1 27. The method of claim 24, further including:
2 fabricating a decoupling capacitor in the processor package.

1 28. The method of claim 24, further including:
2 fabricating a decoupling capacitor in an interposer that is integral
3 with the processor package.

1 29. The method of claim 24, further including:
2 between the DC voltage converter and the STVR, inserting a power
3 socket.

1 30. The method of claim 24, wherein the STVR is disposed in one of a
2 computer, a wireless communicator, a hand-held device, an automobile, a
3 locomotive, an aircraft, a watercraft, and a spacecraft.

1 31. The method of claim 24, wherein an STVR is coupled to at least one
2 of data storage, a digital signal processor, an application-specific integrated circuit,
3 and a microcontroller.